

CLAIMS

1. A process for producing a semiconductor device comprising:

5 a step of forming a gate electrode on a semiconductor substrate by performing a lithographic step using a reticle pattern provided with a substantially linear gate electrode pattern which comprises at least two transistor regions and contact regions formed between these transistors and has paired  
10 first and second long sides and a pair of short sides, wherein a projecting portion in which at least a part of the contact region is arranged is included in the first long side and a concave portion facing at least the entire length of the projecting portion is included  
15 in the second long side facing the first long side between the transistor regions of the reticle pattern.

2. A process for producing a semiconductor device according to claim 1, wherein the length of the concave portion parallel to the second long side is longer than  
20 the length of the concave portion parallel to the first long side and the width of the concave portion parallel to the short side is smaller than the diameter of the contact region.

3. A process for producing a semiconductor device according to claim 1, wherein the gate electrode is  
25 used as a gate electrode of a drive transistor and load transistor which constitute an SRAM memory cell.

4. A process for producing a semiconductor device according to claim 2, wherein the gate electrode is used as a gate electrode of a drive transistor and load transistor which constitute an SRAM memory cell.

5           5. A process for producing a semiconductor device according to claim 1, wherein the gate electrode is used as a transfer transistor constituting an SRAM memory cell, and wherein the conversion to the reticle dimension from a design gate length representing the width of a gate electrode of a transistor having a gate electrode having the same pattern as the convex and concave portions is made such that a gate length representing the width of a gate electrode of the transfer transistor is converted into the reticle dimension in a smaller conversion ratio to a design value.

20           6. A process for producing a semiconductor device according to claim 2, wherein the gate electrode is used as a transfer transistor constituting an SRAM memory cell, and wherein the conversion to the reticle dimension from a design gate length representing the width of a gate electrode of a transistor having a gate electrode having the same pattern as the convex and concave portions is made such that a gate length representing the width of a gate electrode of the transfer transistor is converted into the reticle dimension in a smaller conversion ratio to a design

value.

7. A semiconductor device comprising a semiconductor substrate and a substantially linear gate electrode pattern which is formed on the semiconductor substrate, is provided with two transistor regions and contact regions formed between these transistors and has paired first and second long sides and a pair of short sides, wherein a projecting portion in which at least a part of the contact region is arranged is included in the first long side and a concave portion facing at least the entire length of the projecting portion is included in the second long side facing the first long side between the transistor regions of the gate electrode pattern.

8. A semiconductor device according to claim 7, wherein the length of the concave portion parallel to the second long side is longer than the length of the convex portion parallel to the first long side and the width of the concave portion parallel to the short side is smaller than the diameter of the contact region.

9. A semiconductor device according to claim 7, wherein the gate electrode is used as a gate electrode of a drive transistor and load transistor which constitute an SRAM memory cell.

10. A semiconductor device according to claim 8, wherein the gate electrode is used as a gate electrode of a drive transistor and load transistor which

constitute an SRAM memory cell.

11. A semiconductor device according to Claim 7,  
wherein a drain of the drive transistor is electrically  
connected to a drain of the load transistor through  
5 a metal wiring which is formed directly on the  
semiconductor substrate.

12. A semiconductor device according to Claim 9,  
wherein a drain of the drive transistor is electrically  
connected to a drain of the load transistor through  
10 a metal wiring which is formed directly on the  
semiconductor substrate.

13. A semiconductor device according to Claim 10,  
wherein a drain of the drive transistor is electrically  
connected to a drain of the load transistor through a  
15 metal wiring which is formed directly on the  
semiconductor substrate.